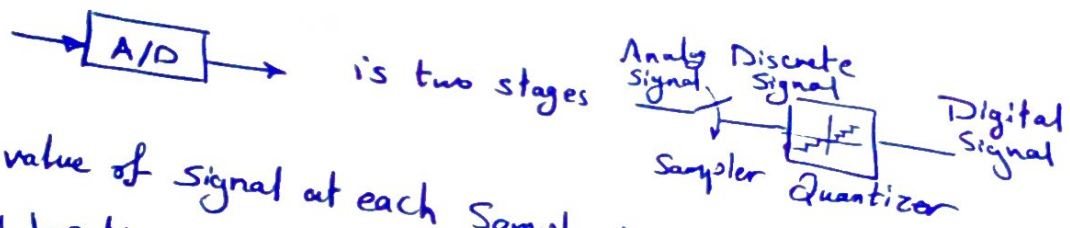


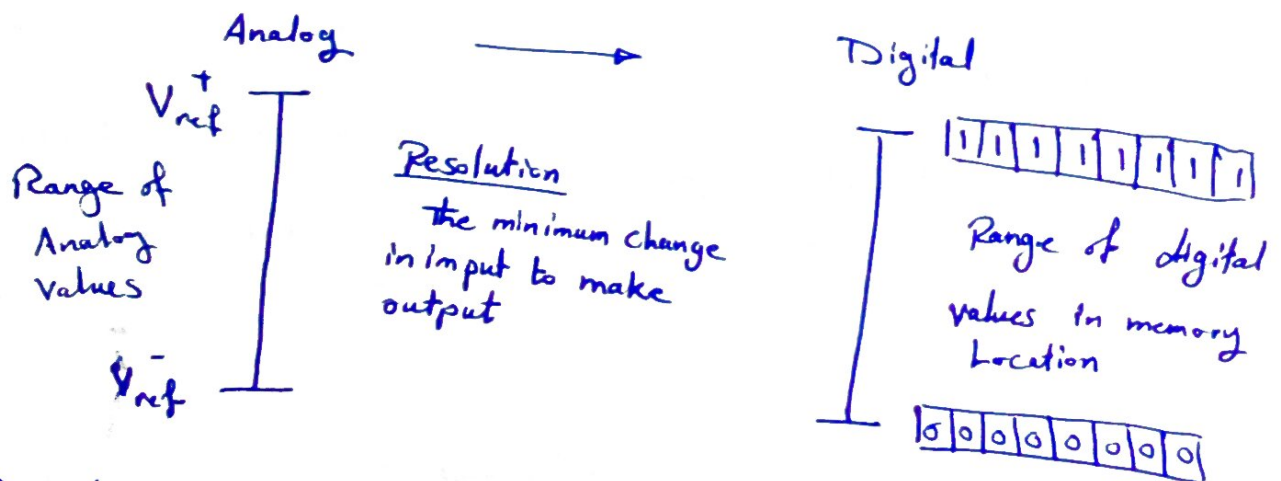
* Analog / Digital Conversion

- Digital Systems require digital input to deal with and generate (produce) digital output. The conversion from Analog world to digital is necessary.
- Our analysis is applied to discrete signals (continuous in amplitude, discrete in time). In practice, using a digital platform to implement digital controller requires signals to be digital (Discrete in both time and amplitude).



- The value of signal at each sample is stored in finite length word (memory location in the Computer System)

* Analog / Digital Conversion equations



A/D resolution: determines the analog value required to increment the value in register by 1

A/D resolution: determined by width of register (n-bits)

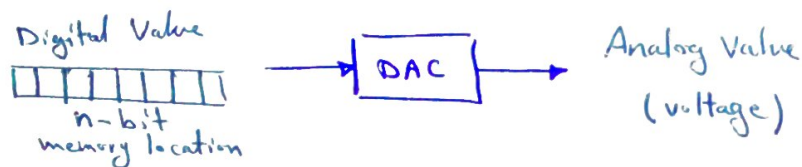
$$\text{Resolution} = \frac{V_{ref}^+ - V_{ref}^-}{2^n - 1}$$

2b Larger n means higher accuracy for A/D converter

$$\text{Analog Value} = \text{Resolution} * \text{Digital Value}$$

* DAC: Digital to Analog Converters

(2)



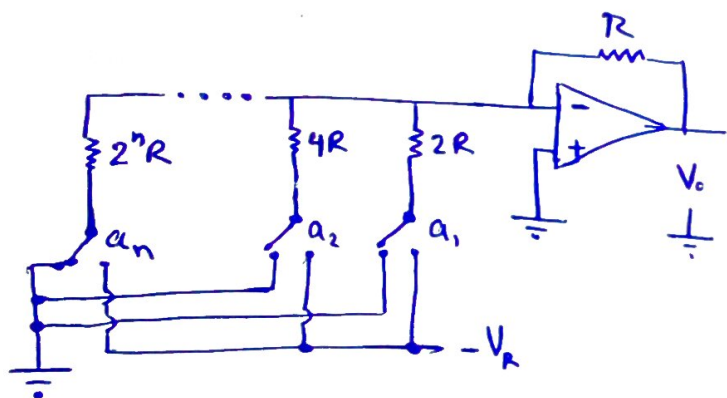
$$V_o = V_R [a_1 2^{-1} + a_2 2^{-2} + \dots + a_n 2^{-n}]$$

where: V_R : reference voltage

V_o : Analog Output Value

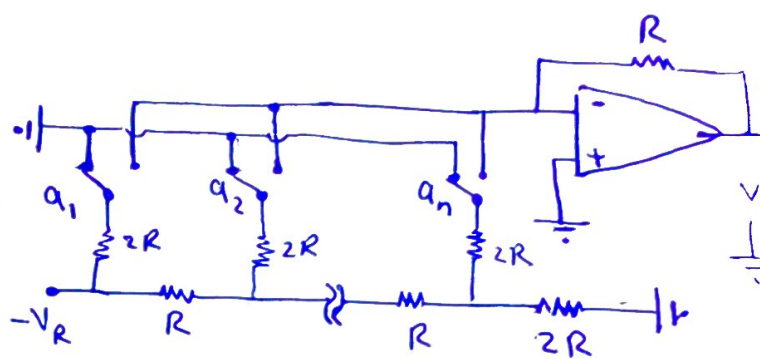
$a_1 - a_n$: Digital Values of bits

a_1 : MSB, a_n : LSB



(Weighted Resistor DAC)

- Requires large number of different values of resistors (Disadvantage)

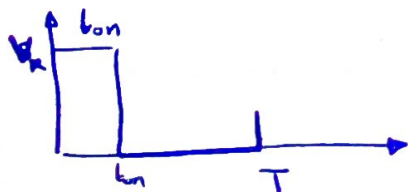


(Inverted R-2R ladder)

Requires Only two different values of resistors

* DAC vs. PWM

PWM: Pulse Width Modulation



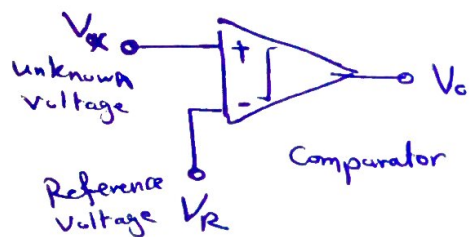
The output has two cases 0 or V_R -volt (Digital) but t_{on} is changed

$$V_{avg} = \frac{1}{T} \int_0^T V(t) dt = \frac{1}{T} \int_0^{t_{on}} V_R dt + 0$$

$$V_{avg} = \frac{t_{on}}{T} V_R = k V_R, \quad k = \text{duty cycle (0-1)}$$

* ADC : Analog to Digital Converters

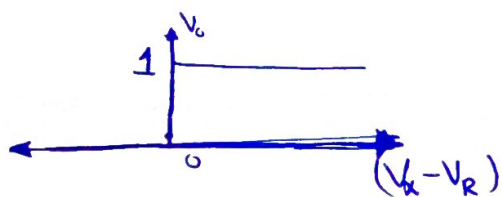
Basic Idea : Compare unknown voltage with Reference voltage to determine level (Binary levels)



V_R is varied to determine which of 2^n possible binary words is closest to V_x .
 V_R can assume 2^n different values of the form

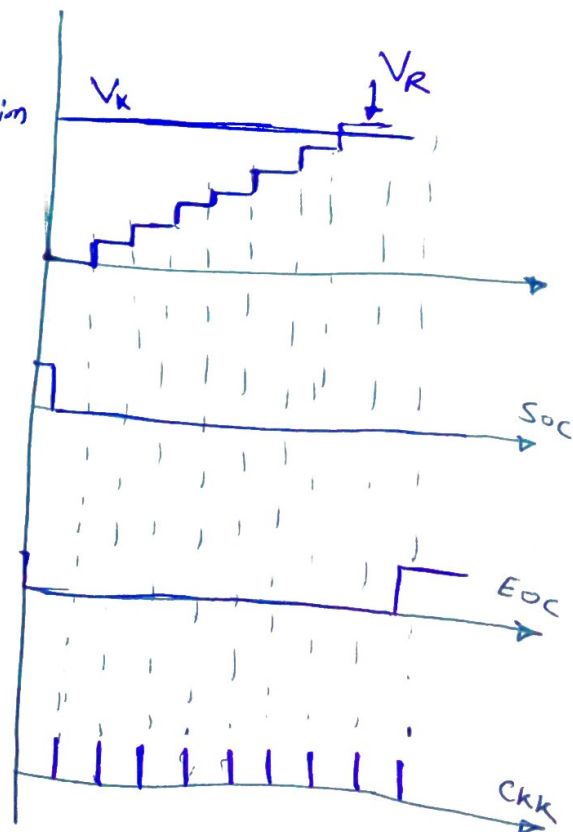
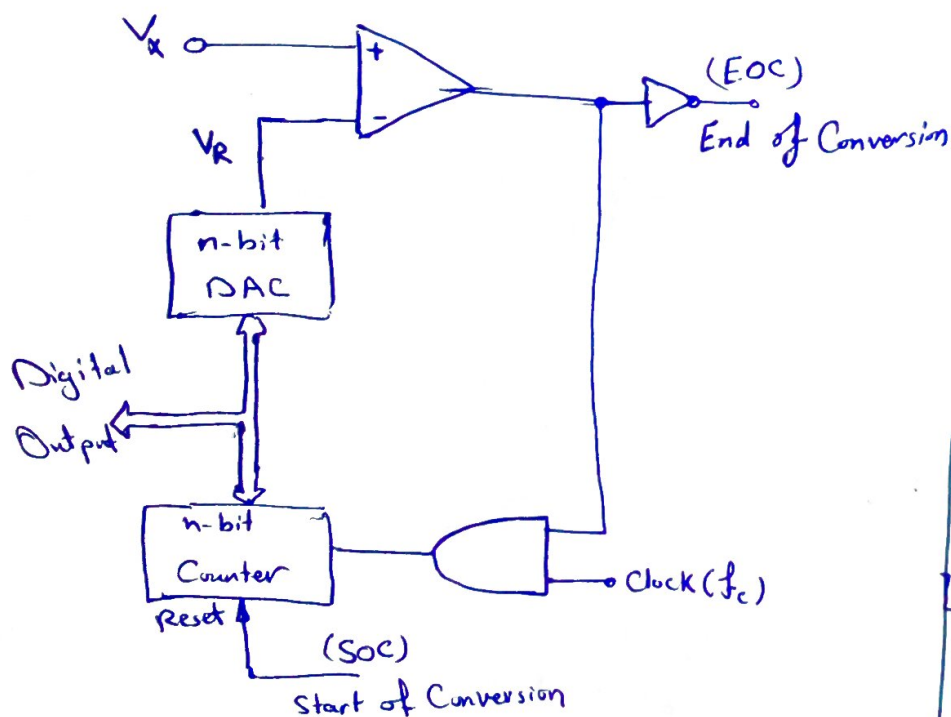
$$V_R = V_r \sum_{i=1}^n A_i 2^{-i}$$

V_r : DC reference Voltage
 A_i : Binary Coefficients

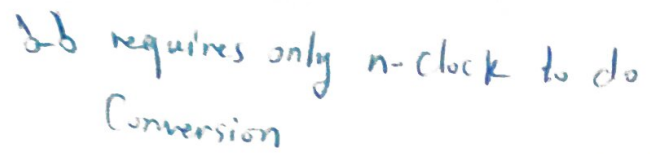


So A_i are choosed so that $\text{error} = |V_x - V_R| = |V_x - V_r \sum_{i=1}^n A_i 2^{-i}|$ be minimal

① Counter Ramp Converter

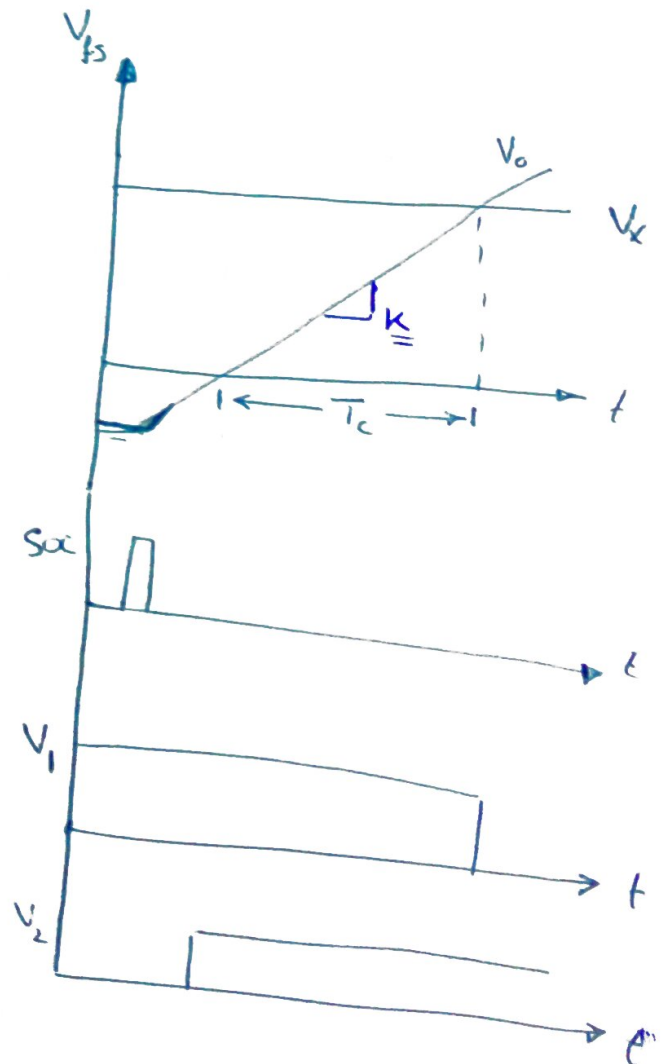


So Requires multiple clocks to do Conversion



$V_r = K T_c = k \frac{N}{f_c}$
 Let $k = V_{ref} \cdot T_c$

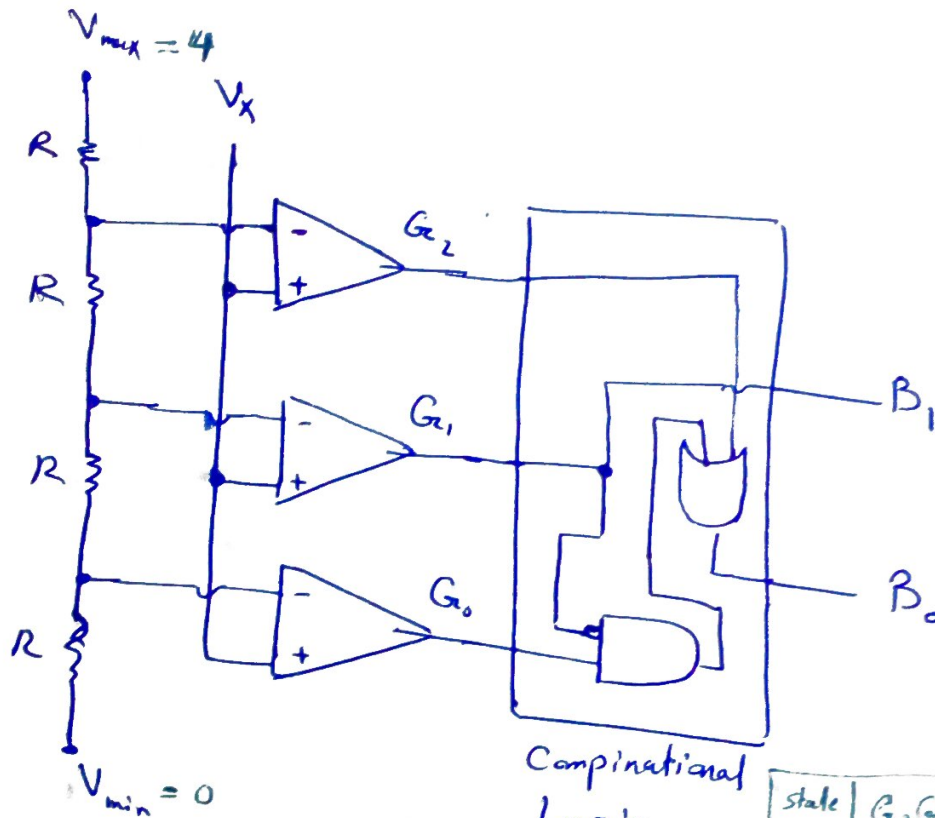
$$V_x = \frac{V_{is} N}{2R}$$



④ Parallel Converter (Flash)

⑤

- use additional Hardware to perform Parallel rather than Serial Conversion
- Fastest Converter
- V_x is Simultaneously Compared to different reference values



2-Bit
Converter

Combinational
Logic
Circuit

$$B_0 = G_0 \overline{G_1} + G_2$$

$$B_1 = G_1$$

state	$G_2 G_1 G_0$	$B_1 B_0$	Voltage
0	000	00	0 - 1
1	001	01	1 - 2
2	011	10	2 - 3
3	111	11	3 - 4

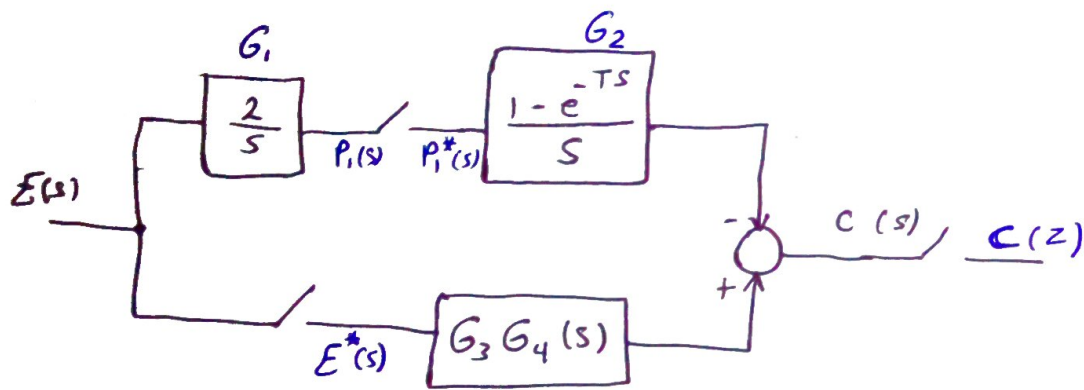
Another Types of ADC :

- Tracking ADC
- Dual Ramp Converter

* Reference :

C. L. Phillips, H. Troy Nagle, "Digital Control System Analysis and Design", 3rd edition - Chapter 3 - Sections 3.8, 3.9

Section 3

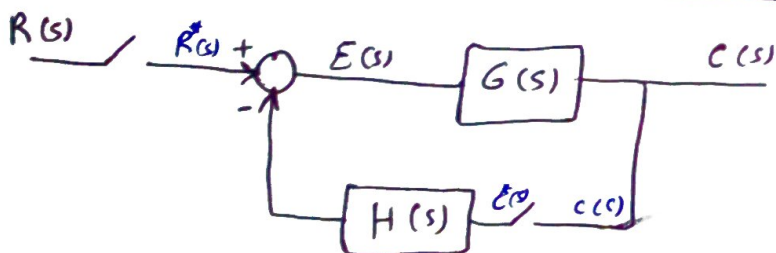


$$C(s) = E^*(s) G_3 G_4(s) - G_2 P_1^*(s)$$

$$P_1(s) = E(s) G_1(s) \rightarrow P_1^*(s) = \overline{G_1(s) E(s)}^*$$

$$C(s) = E^*(s) G_3 G_4(s) - G_2^*(s) \overline{E G_1(s)}^*$$

$$C^*(s) = E^*(s) \overline{G_3 G_4(s)}^* - G_2^*(s) \overline{E G_1(s)}^*$$



$$C(s) = G(s) E(s)$$

$$E(s) = R^*(s) - C^*(s) H(s)$$

$$C(s) = G(s) [R^*(s) - C^*(s) H(s)]$$

$$C^*(s) = G^*(s) R^*(s) - C^*(s) \overline{G H(s)}^*$$

$$(1 + \overline{G H(s)}^*) C^*(s) = G^*(s) R^*(s)$$

$$\frac{C^*(s)}{R^*(s)} = \frac{G^*(s)}{1 + \overline{G H(s)}^*}$$